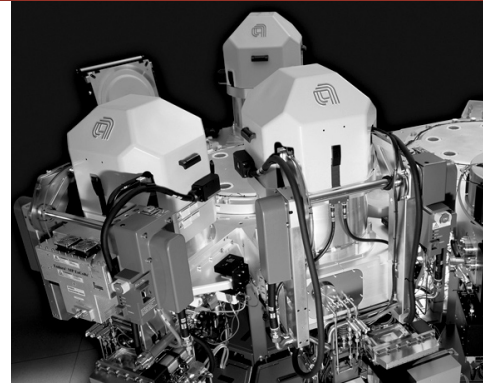


APPLIED ENDURA®/ENDURA2™ CU BARRIER/SEED SYSTEM

≤45nm PVD CU BARRIER/SEED
FOR COPPER METALLIZATION



Cu barrier/seed metallization imposes critical requirements on all four steps of the process sequence: degas, preclean, barrier and Cu seed. Degas removes condensed water or volatile contaminants, leading to good film adhesion and compatibility with low k interlayer dielectrics. Preclean, the second step, cleans the underlying metal interface to remove residues and native oxide. The barrier prevents the diffusion of Cu into the dielectric with a film that provides minimal bottom coverage, good sidewall coverage and no overhang. In addition, the barrier provides good adhesion to Cu.

The Cu seed film, deposited in the final step, is thin and conformal with smooth morphology and no overhang, providing a good nucleation layer for void-free electroplating. The entire process sequence demands excellent temperature control. These requirements intensify with each advancing technology node. Added to these technical requirements are high productivity and low CoC for cost-effective wafer fabrication.

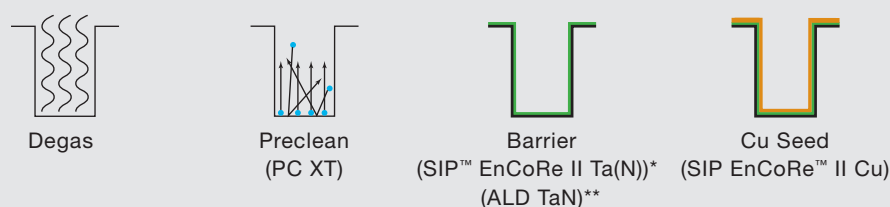
FEATURES

- SIP™ EnCoRe II Ta(N) barrier, in-situ TaN/Ta deposition with re-sputtering through decoupled plasma source
- SIP EnCoRe II Cu seed with optimized source and industry first magnet spacing compensation (MSC) technology
- Dual mode preclean with Ar sputter and reactive capability
- Ultra-thin (<15Å) ALD TaN barrier compatible with advanced low k dielectrics

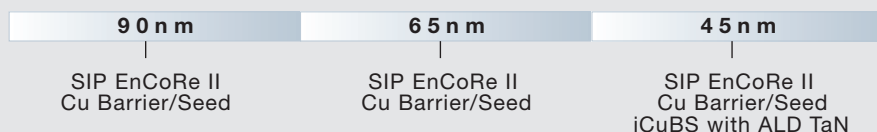
BENEFITS

- Ultra thin and conformal barriers (<100Å) enable low line resistance with robust SM and EM
- Tunable via to trench etch selectivity
- Excellent seed coverage for wide ECP fill window
- Full-face target erosion for long target life (>20,000 wafers), low CoC & CoO
- Clean via bottoms with complete reduction of CuO

Cu BARRIER/SEED PROCESS SEQUENCE



Cu BARRIER/SEED ROADMAP



() Denotes chamber technology

* SIP Encore II system

** iCuBS system

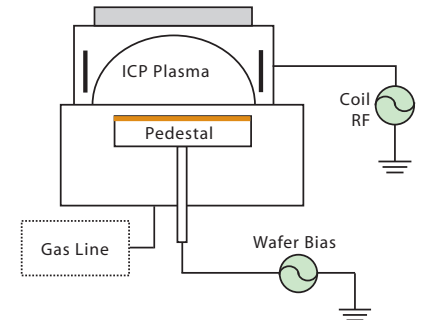
PC XT TECHNOLOGY— SPUTTER AND REACTIVE ETCH IN SINGLE CHAMBER

The PC XT chamber operates in dual mode, providing a reliable single-chamber solution for both physical sputter and reactive clean. The chamber features an enhanced XT process kit for improved performance, and a cooled resonator for efficient thermal management of the bell jar. The PC XT has an option for a Semi S2 CE compliant gas box for reactive clean with high hydrogen concentration capability.

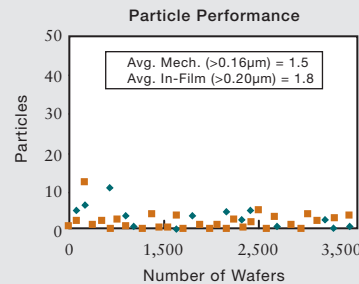
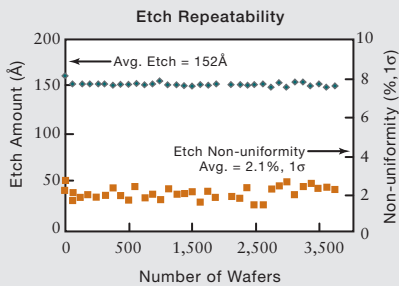
The PC XT Rev 1 oxide process kit eliminates defect sources and has a long kit life. Its robust design improves overall chamber reliability. The chamber uses dual RF sources for independent control of the plasma and sputter energies. The PC XT Rev 2 SiON* process kit has an extended cathode that helps increase kit life for sputtering of high stress materials including SiON, Si₃N₄ and silicide applications.

*and other high stress materials

PC XT CHAMBER DESIGN



300mm SiON



Preclean solution for both SiO₂ and SiON oxide films.

SELF-IONIZED PLASMA (SIP) ENHANCED COVERAGE BY RE-SPUTTERING (EnCoRe II) SYSTEM

To extend the manufacturing requirements of PVD to 45nm technology generations and beyond, Applied Materials provides the SIP EnCoRe II Ta(N) barrier and SIP EnCoRe II Cu seed. SIP EnCoRe II Ta(N) barrier provides thin conformal barrier films that enable customers to lower barrier thickness for line resistance scaling to 45nm. The high plasma density magnetron has increased sidewall coverage to >25% on 65nm structures improving stress migration and electromigration reliability. SIP EnCoRe II Cu seed improves uniformity and sidewall coverage with an optimized source and side magnets leading to a wider ECP fill window. The industry first magnets spacing compensation technology enables stable process performance over 30,000 wafers. The SIP EnCoRe II chambers are integrated with Preclean (PC) XT chambers, providing reactive and sputter etch via clean capabilities.

Barrier/seed chambers come standard with Super Low Temperature E-Chucks (SLT-ESC), providing full coverage deposition with low temperature capability for a smooth conformal film. The ceramic SLT-ESC enables high throughput with fast de-chucking. The SIP EnCoRe II Cu barrier/seed system on the Applied Endura/Endura2 platform offers exceptional reliability, while maintaining high throughput (>80wph) for today's Cu interconnect production.

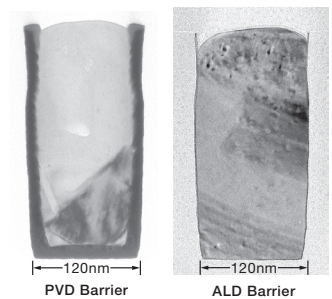
Proven parametric and reliability data from Applied Materials' Dan Maydan Technology Center using state-of-the-art 90nm and 90nm shrink structures validates process development with the SIP EnCoRe II barrier/ seed SM data on aggressive 90nm shrink structures with large metal pads above and below 0.11 μ m vias show virtually no shift in Rc and Rc distribution. EM data on 90nm shrink structures show extrapolated lifetime ($t_{0.1}$) at 105°C exceeds the specification of 10 years. SIP EnCoRe II processes for barrier and seed are optimized for the best parametric and reliability results with low k Black Diamond™ dielectrics.

INTEGRATED Cu BARRIER/SEED (iCUBS™) SYSTEM

Enabling ≤ 65 nm technology, the Endura iCuBS system features ALD TaN barrier with SIP EnCoRe II Cu PVD seed on the industry-leading Endura XP mainframe.

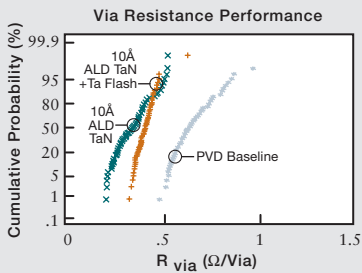
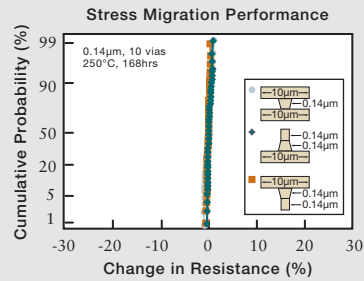
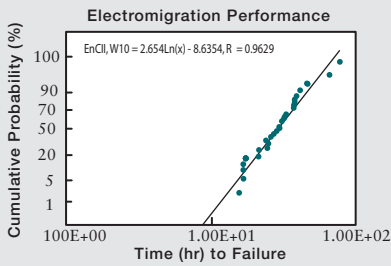
Applied Materials' breakthrough TaN barrier takes advantage of ALD technology—ultra thin film deposition one atomic layer at

Cu Interconnect Cross Sections

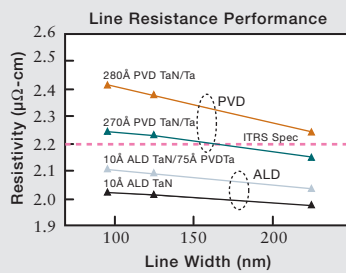


ALD TaN minimizes barrier cross section enabling lower interconnect resistance

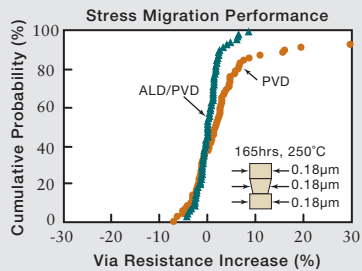
PROVEN INTEGRATION AND RELIABILITY



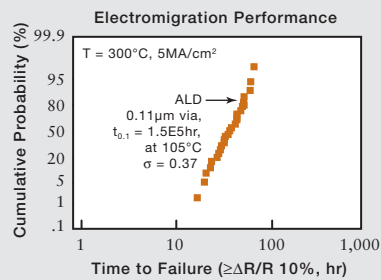
Low via resistance with ALD TaN compared to PVD baseline



ALD TaN enables consistently low interconnect line resistance



Stress migration with Black Diamond II exhibits equivalent reliability to PVD



Excellent EM performance on aggressive features sizes. T>10 years at 105°C and 5MA/cm² testing current

a time with precise thickness control—to deliver 100% conformal step coverage with good particle performance. ALD TaN is an effective barrier with advanced low k dielectrics, including Black Diamond, and integrates fully with ECP and CMP processes.

The conformal ALD TaN barrier combined with SIP EnCoRe II Cu PVD seed results in low overhang, enabling void-free Cu fill.

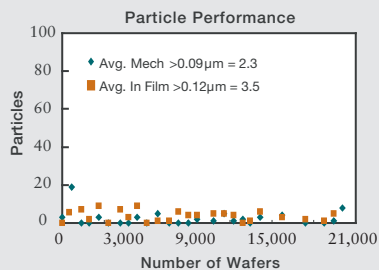
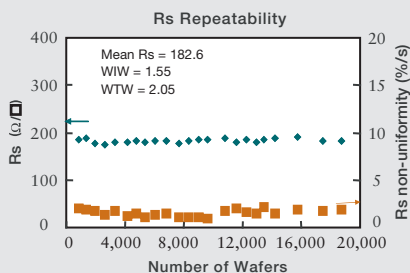
Thin ALD TaN films are essential for line resistance scaling as device dimensions shrink below 65nm. Parametric data clearly shows ALD TaN films will meet ITRS resistivity specifications for these generations. Data from Applied Materials' Dan Maydan Technology Center shows 10Å of ALD TaN exhibits lower resistance per via than conventional PVD while providing equivalent reliability performance in aggressive stress migration tests.

SIP EnCoRe II Ta(N) II BARRIER TECHNOLOGY

SIP EnCoRe II Ta(N) barrier technology is an advanced PVD solution for in situ TaN/Ta and Ta barrier deposition. SIP EnCoRe II Ta(N) barrier uses a proprietary dual-mode capability for barrier film deposition: an ionized PVD deposition mode for enhancing sidewall coverage, and an ICP mode for re-sputtering to improve sidewall coverage and reduce bottom coverage. The new high plasma density magnetron allows for >25% barrier sidewall on 0.1μm (65nm) vias allowing customers to reduce the effective barrier thickness as low as 100Å. This allows for decreased line resistance enabling 65 and 45nm requirements. Electromagnets on the SIP EnCoRe II Ta(N) independently control deposition at etch uniformity to <3%, 1σ for the tightest Rc distribution.

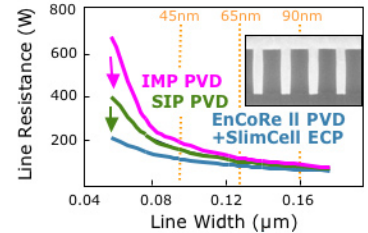
The enhanced process kit hardware provides excellent particle control throughout target life, demonstrating repeatable process performance in a production-proven design. The decoupled plasma source allows for selective etch which allow Punchthru™ of the via while still protecting the trench bottom.

The SIP EnCoRe II Ta(N) chamber design features a flat Ta target (1) which enables low defects, in situ TaN/Ta deposition and low COC, an advanced magnetron design (2) to enhance ionization, the SLTESC with high bias capability (3), a Ta coil (4) for re-sputtering, ensuring soft Ar⁺ ion selective etch capability and electromagnets (5) for independently tuning deposition and etch uniformity. The SLT-ESC with temperature control maintains low wafer temperature uniformity across the wafer surface.

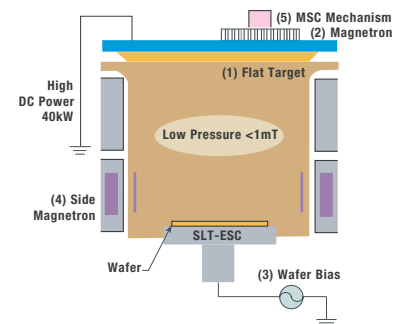


Production-proven hardware delivers low non-uniformity and low in-film and mechanical defects of SIP EnCoRe II Ta(N) with bi-layer resputter process

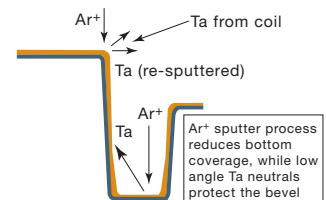
Metallization Conformality, Scaling and Reliability



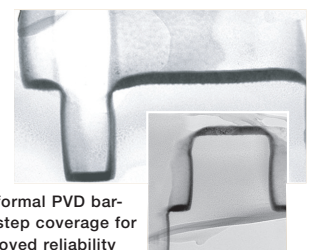
SIP EnCoRe II Ta(N) Chamber Design



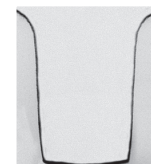
Tunable Coverage (Low Bottom, High Sidewall)



SIP EnCoRe II Ta(N) Barrier



Conformal PVD barrier step coverage for improved reliability



Thin and conformal 40Å PVD barrier for low line resistance

ALD TaN BARRIER TECHNOLOGY

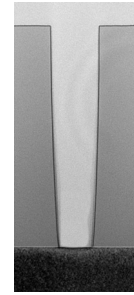
ALD TaN barrier technology is an advanced barrier solution to meet the needs of the 65nm and below technology nodes. This enabling capability allows for low via and line resistance. ALD TaN has proven reliability on Black Diamond II dielectrics, and demonstrated good stress migration resistance at 250°C for 168hrs.

The ALD TaN product utilizes a compact, advanced chamber design (1) for faster cycle times and a low temperature process with a wide process window (50°C). The small volume chamber (2) enables high throughput of 30wph (for 10Å film). The proprietary chamber design enables efficient gas usage thereby lowering CoC. The ALD TaN chamber along with its low CoC and high throughput facilitates low CoO and production worthiness.

SIP EnCoRe II CU SEED TECHNOLOGY

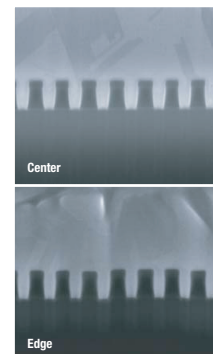
SIP EnCoRe II Cu seed delivers high performance PVD solution for 45nm Cu seed applications. With enhanced chamber hardware, SIP EnCoRe II Cu provides excellent uniformity and particle control throughout target life. A high plasma density magnetron provides conformal seed sidewall coverage ensuring a wide ECP gapfill window down to 300Å of seed thickness. An industry first magnet spacing compensation technology coupled with a unique magnet rotational mechanism has enabled 2X target life on the SIP EnCoRe II Cu chamber with stable process performance over 30,000 wafers.

ALD TaN Barrier Conformal Coverage



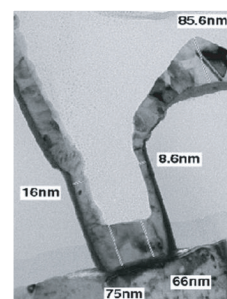
200nm x 1.20μm via, 15 Å ALD thickness, 100% step coverage

SIP EnCoRe II Cu Bottom Coverage



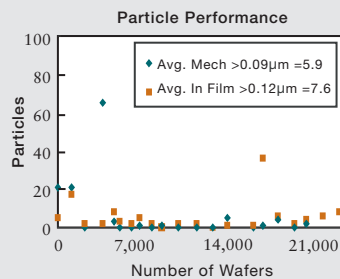
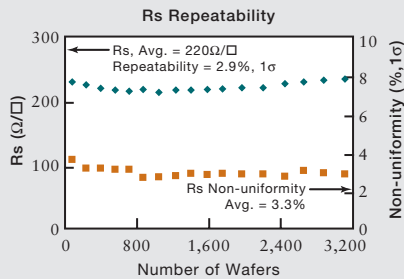
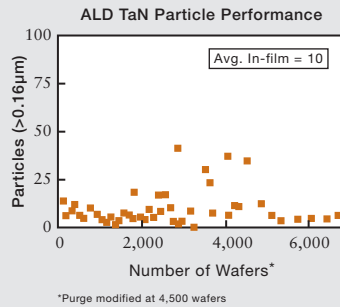
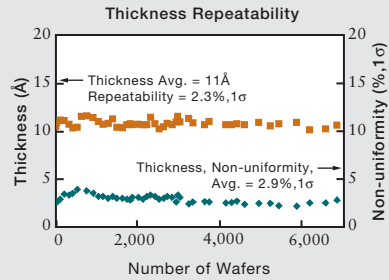
Void-free gap-fill on 45nm trench, 0.055μm, 4:1 A/R

SIP EnCoRe II Cu Bottom Coverage



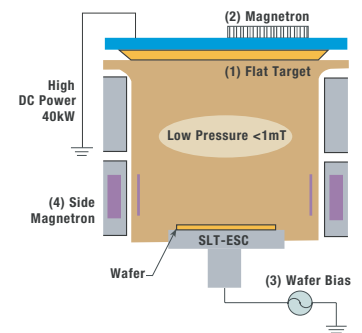
60% bottom coverage, 95Å minimum sidewall thickness and <2:1 asymmetry on 0.25μm, 4:1 A/R structure

DEMONSTRATED PERFORMANCE



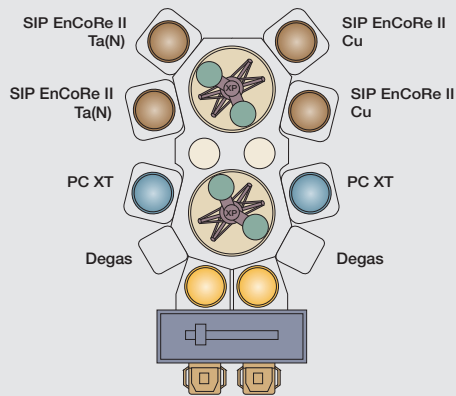
Similar to the SIP EnCoRe II barrier chamber, the SIP EnCoRe II Cu chamber design features a flat Cu target (1) for low CoC, advanced magnetron design (2) to enhance ionization, the SLT-ESC with high bias capability (3), and flux shaping side magnets (4) for good film uniformity and step coverage. The SLT-ESC maintains wafer temperature control at <50°C to prevent Cu agglomeration along the sidewalls of the via. High bias capability helps to control re-sputtering efficiency for a more conformal deposition.

SIP EnCoRe II Cu Chamber Design



CU BARRIER/SEED BKM CONFIGURATION

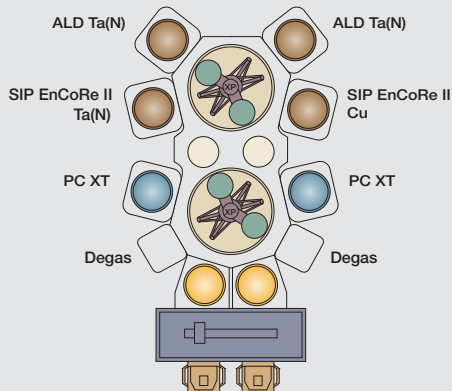
Applied Endura/Endura2 300mm
Cu Barrier/Seed PVD



Throughput >80wph

iCUBS BKM CONFIGURATION

Applied Endura/Endura2 300mm
iCuBS ALD/PVD



Throughput >60wph

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